SUBHARTI INSTITUTE OF TECHNOLOGY & ENGINEERING

(College established in 2005 & Approved by AICTE)

0121-2439043/52, Fax: 0121-2439067, E-mail: engineering@subharti.org, Web: www.engineering.subharti.org

A constituent college of

SWAMI VIVEKANAND SUBHARTI UNIVERSITY

(Established under U.P. Govt. Act no. 29 of 2008 and approved under section 2(f) of UGC Act 1956)

Department of Electronics & Communication Engineering

Ref. No/SITE/ECE/DA/DA/2019/I(A)

Dated: 25-09-2019

NOTICE

The Department of ECE in association with SITE is organizing the Blended Learning Course name as Value Added Course on "VERILOG" at Subharti Institute of Technology and Engineering, Swami Vivekanand Subharti University, Meerut. The course classes are scheduled to be conducted from 7th -21st, October, 2019. This course will enhance the practical skills and make student exposure to Verilog RTL Design with various EDA tools used in the field of electronics. The proposed course will be open for ECE & EEE students on the basis of first come first serve. This course will be coordinated by Er. Rajesh Parihar, Assistant Professor, Department of ECE, SITE. There are no charges for the course.

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Important Dates:

- Last date for receipt of application- 30th September, 2019
- Last date for acceptance application- 5th October, 2019

CC:

- Principal
- Department of EEE

Encl:

- Registration form

Registrar
Swami Vivekanand
Subharti University
MEERUT

HOD (ECE) 25/09/2019

Syllabus:

Module	Particulars	Contact Hours
1	Module 1: RTL Design Using Verilog : Introduction, Verilog Naming convention, Operator in Verilog , Verilog Data Types, Numbers in Verilog, Behavioral modeling, structural modeling, Delay modeling in Verilog, UDP, Assignment Statements, Sequential Block, Wait Statement, Procedures in Verilog, Control Statement, Loop Statement, If statement, Combinational Logic in Verilog, Sequential Logic in Verilog, FSM in Verilog, Test Benches in Verilog, Example Designs in Verilog, Moore and Mealy Machine, Selected References.	9
2	Module 2: Xilinx ISE EDA Tool and Microwind Tool	3
3	Module 3: Lab sessions using Xilinx ISE and Microwind Tool: 3.1 SIMULATION OF ARITHMATIC LOGIC UNIT 3.2 STUDY OF IMPLEMENTATION IN FPGA 1. IMPLEMENTATION OF HALF ADDER AND FULL ADDER IN FPGA	3

Course Description

The Verilog Language and Application course offers a comprehensive exploration of the Verilog HDL and its application to ASIC and programmable logic design. The course provides a solid background in the use and application of the Verilog HDL to digital hardware design. This training course covers all aspects of the language, from basic concepts and syntax through synthesis coding styles and guidelines to advanced language constructs and design verification. It also touches upon ASIC library design concepts.

- **Learning Objectives**

After completing this course, you will be able to:

- Use fundamental Verilog constructs to create simple designs
- Ensure that Verilog designs meet the requirements for synthesis
- Develop Verilog test environments of significant capability and complexity

Software Used in This Course

- Xilinx Tool 10.2 ISE
- Microwind Tool version 3

Modules in this Course

- Describing Verilog Applications
- Language Introduction

- Choosing Between Verilog Data types
- Using Verilog Operators
- Making Procedural Statements
- Using Blocking and Non-Blocking Assignments
- Using Continuous and Procedural Statements
- Understanding the Simulation Cycle
- Using Functions and Tasks
- Directing the Compiler
- Introducing the Process of Synthesis
- Coding RTL for Synthesis
- Designing Finite State Machines
- Avoiding Simulation Mismatches
- Managing RTL Coding Process
- Managing the Logic Synthesis Process
- Coding and Synthesizing an Example Verilog Design
- Using Verification Constructs
- Coding Design Behavioral Algorithmically
- Using System Tasks and System Functions
- Generating a Test Stimulus
- Developing a Testbench
- Example Verilog Testbench

Audience

- Second Year and Pre-final Year B.Tech students.

Prerequisites

You must have knowledge of the following:

- How to navigate a file system and use a text editor
- A basic understanding of digital hardware design and verification.

Hand on and Course Outcome

Hardware Description language such as Verilog are similar to software languages because that include ways of describing the propagation time and signal strengths (sensitivity). There are two types of assignments operators we have taught and students have learned about a blocking assignment and non blocking assignment.

- **Scope and Limitation:**

Verilog has its vast scope with AMS –Analog Mixed signals. Hand on was done along with simulation for Verliog Value added courses Scope of this value added course is that it can be used as a learning platform for industry based projects. This course has limitation that we have not covered Analog and Mixed Simulation in it which can be done at advance level.

Subharti Institute of Technology and Engineering
Swami Vivekanand Subharti University, Meerut
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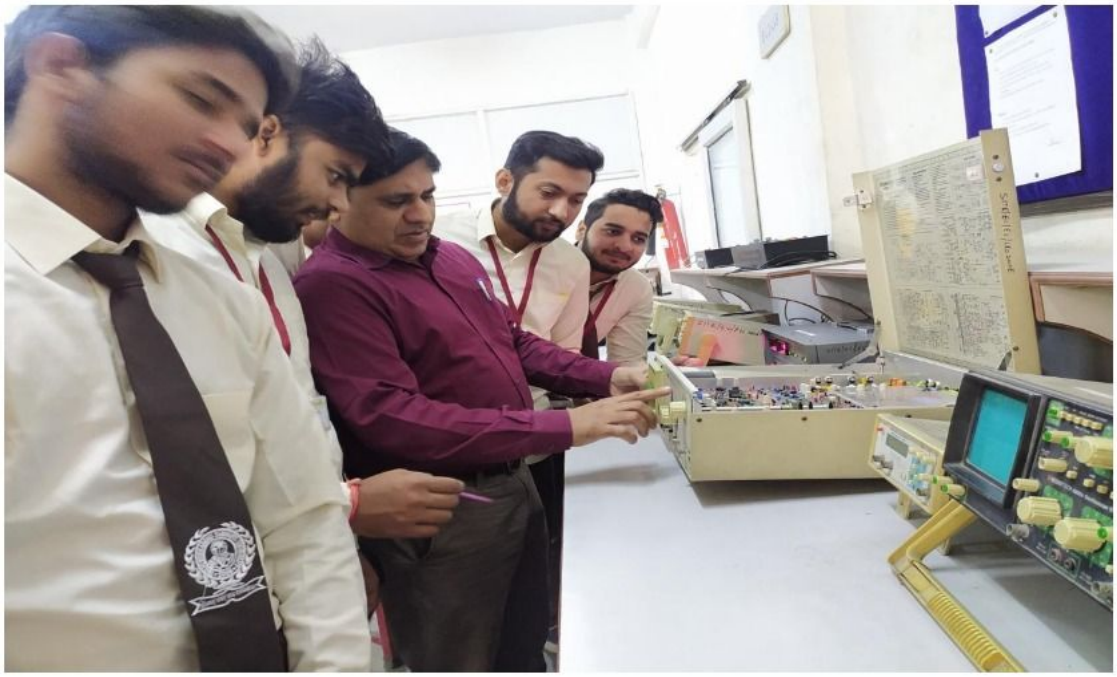
Report on Value Added Course
"VERILOG"

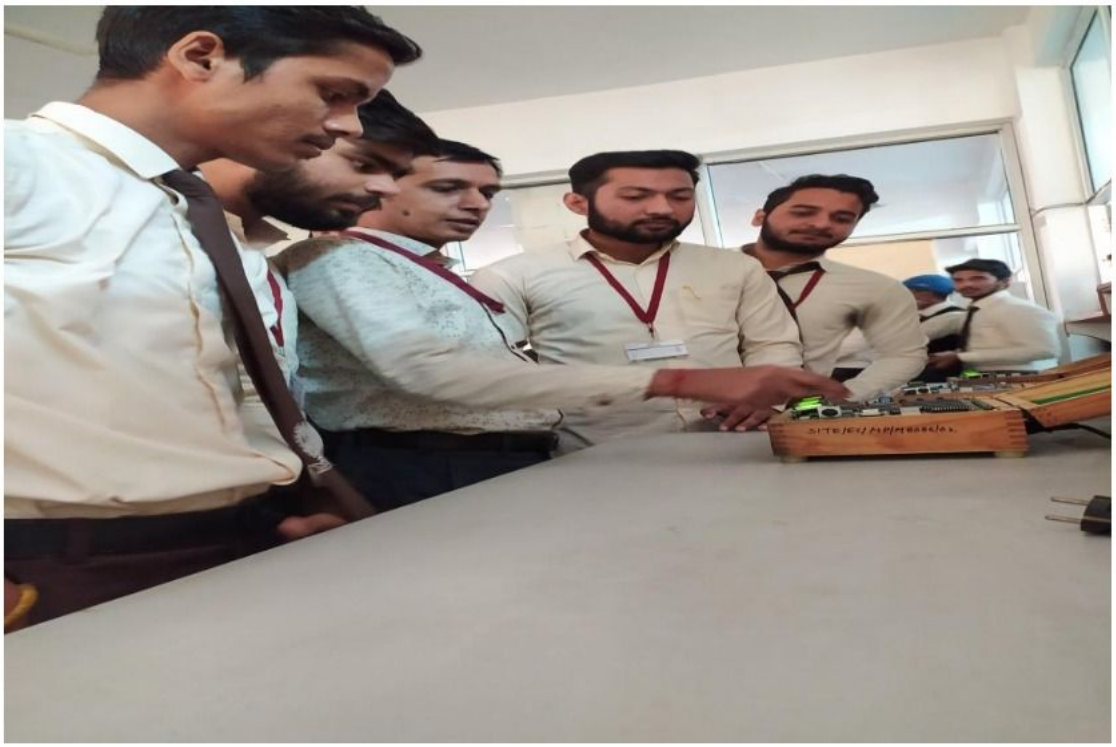
The department of ECE in association with SITE organized a Value Added Course on **"VERLOG"** was started from 7th Oct, 2019 till 21th Oct 2019 at room no. 209 1st floor SITE, SVSU, Meerut. A total of 6 participants participated in this course. The purposed course will be coordinated by Er. Rajesh Parihar (Assr. Prof.). The main aim to introduce this course was to improve students' tolerance for ambiguity; improve reflective skills and self-awareness which are particularly relevant to the role of professional person.

COURSE OBJECTIVES:

This course will enhance the practical skills and make students exposure to Verilog RTL design with various ETA tools used in the field of electronics.

Registrar
Swami Vivekanand
Subharti University
MEERUT





Students during Value Added Course Session

Subharti Institute of Technology and Engineering
Swami Vivekanand Subharti University, Meerut
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SESSION: 2019-20

COURSE NAME: VERLOG
COURSE CODE: ET-VA-19

LIST OF STUDENTS

S.NO	NAME OF STUDENT
1	Maheshwar Narayan
2	Zubair Khan
3	Lalrinfela
4	Rahul Kumar Anand
5	Avinash Yadav
6	Ankur Malik

PRINCIPAL

Registrar
Swami Vivekanand
Subharti University
MEERUT