VAC Name: VERLOG
(ET-VA-12)

Subharti Institute of Technology and Engineering
Swami Vivekanand Subharti University, Meerut
(Approved by AICTE)
Subhartipuram, NH-58 Delhi-Haridwar Bypass Road, Meerut-250005 (U.P.)
Ph.: 0121-2439157, Ext. 2222, 2221, Fax: 0121-2439108
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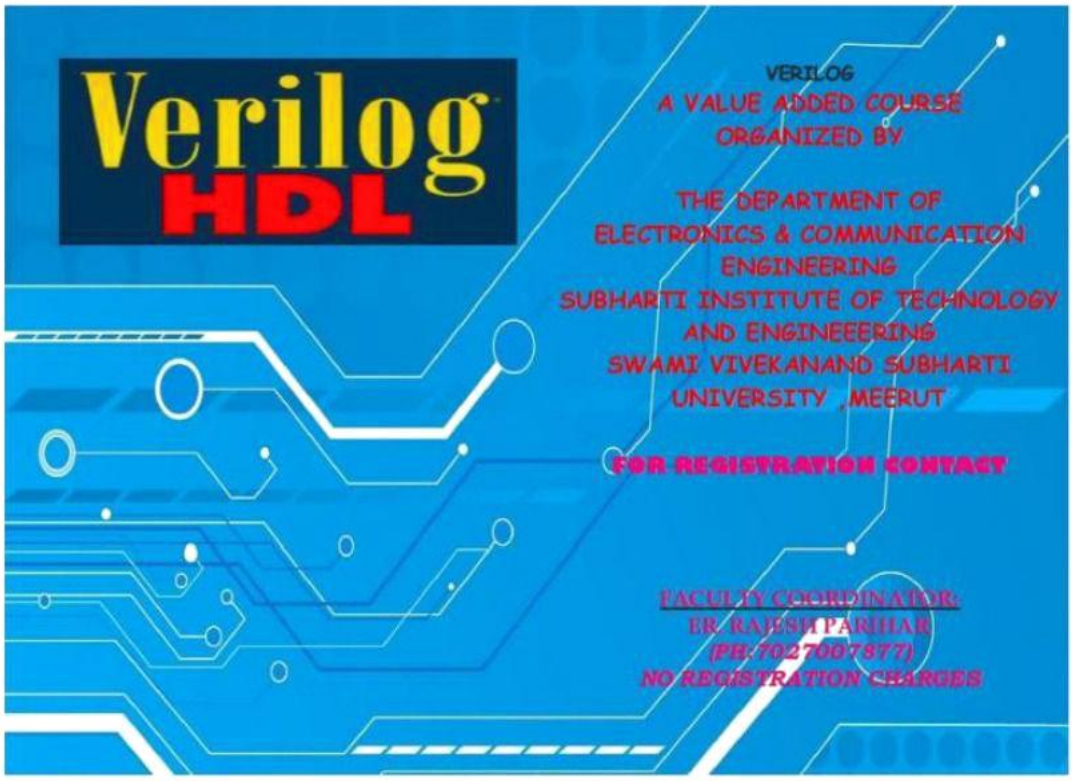
VALUE ADDED COURSES

SESSION : 2018-19

COURSE NAME: VERLOG
COURSE CODE: ET-VA-12

1. **BROCHURE**



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2. REGISTRATION FORM:

REGISTRATION ELIGIBILITY

For all UG-PG students of ECE, EEE & CS/IT .
No registration fees.

HOW TO REGISTER

Interested participants should send their duly completed registration form through their respective Head of the Departments to Mr Rajesh Parihar,Asst. Prof.,ECE for registering their names as a participant in the "VALUE ADDED COURSE ON VERILOG " organized by Department of Electronics & Communication Engineering ,SITE, SVSU , Meerut.The participants need to submit individual entry forms.

IMPORTANT DATES

Last date for receipt of application:
29th September 2018
Last date for acceptance notification:
2nd October 2018

VENUE

Room no 209 1st floor
Subharti Institue of Technology and Engineering, SVSU, Meerut

PATRON

Dr. Bikas Prasad
Principal, SITE

Er. Amit Kumar
HoD, ECE

CO-ORDINATOR
Er. Rajesh Parihar, Asst Prof(ECE),SITE
Mob: +917027007877
Email : parihar.rajesh@gmail.com

FPGA
FPGA Chip
V E R I L O G

VALUE ADDED COURSE
ON

VERILOG

03RD OCTOBER 2018 -17TH OCTOBER 2018

Organized by:
Department of
Electronics & Communication Engineering,
Subharti Institute of Technology and Engineering

SWAMI VIVEKANAND
SUBHARTI UNIVERSITY
MEERUT

Course Contents

Module	Particulars	Contact Hours
1	**Module 1: RTL Design Using Verilog :** Introduction, Verilog Naming convention, Operator in Verilog , Verilog Data Types, Numbers in Verilog, Behavioral modeling, structural modeling, Delay modeling in Verilog, UDP, Assignment Statements, Sequential Block, Wait Statement, Procedures in Verilog, Control Statement, Loop Statement, If statement, Combinational Logic in Verilog, Sequential Logic in Verilog, FSM in Verilog, Test Benches in Verilog, Example Designs in Verilog, Moore and Mealy Machine, Selected References.	9
2	**Xilinx ISE EDA Tool and Microwind Tool**	3
3	**Lab seesions using Xilinx ISE and Microwind Tool:** 3.1 **SIMULATION OF ARITHMATIC LOGIC UNIT** 3.2 **STUDY OF IMPLEMENTATION IN FPGA** 3.3 **IMPLEMENTATION OF HALF ADDER AND FULL ADDER IN FPGA**	8

COURSE OUTCOMES:

1. Students should be able to understand the Verilog Hardware Description language to synthesis real world hardware using digital circuits.
2. Student should be able to understand the concept Register Transfer Level coding style in Verilog HDL.
3. Students should be able to know the Digital design flows and design trade-offs.
4. Students will gain to work on Modelsim simulation environment.
5. Students will get concept of Test bench construction.
6. Student should be learning the implementation of simple digital logic using FPGA SPARTAN 3E hardware kits. Realisation of all above concepts in hardware designs.

TEXT BOOKS:

1. Samir Palnitkar- "Verilog HDL- A Guide to Digital Design" Sunsoft Press, 1996
2. Debaprasad Das- "VLSI Design Oxford University Press, Second Edition" 2014

REPORT ON VALUE ADDED COURSE ON VERILOG

ET VA 12

Verilog HDL is used as Electronic Design Automation language. This is used in Hardware Description language as an counter to VHDL.

Agenda

- What is Verilog?
- Tools Support
- Synthesis and simulation
- Objectives of Verilog.

What is Verilog :

Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using a HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.

Verilog supports a design at many levels of abstraction. The major three are −

- Behavioral level
- Register-transfer level
- Gate level

Tools Support:

1. Xilinx ISE 10.1i
2. Microwind 3
3. Altera

Synthesis Tools and Simulation:

1. Mentor Graphics
2. ISIM

Objective of Verilog:

This course will provide an overview of the Verilog with the following objectives:

- Explain design, test and implementation of digital hardware
- Explain the hierarchy and modeling of structures
- Introduces syntax, lexical conventions, data types and memory
- Behavioral and register transfer level modeling

Demonstration given on hardware

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VALUE ADDED COURSES

SESSION : 2018-19

COURSE NAME: VERLOG
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LIST OF STUDENTS ENROLLED FOR VALUE ADDED COURSE

S.NO.	ENROLL NO.	NAME OF STUDENTS
1.	1501010000927	AQEEDAT HUSSAIN
2.	1501010000935	VISHAL CHAUDHARY
3.	1501010000928	ANKUR YADAV
4.	1601010000388	VARSHA SHARMA
5.	1601010000302	NISHESH GUPTA
6.	1701010001337	HARSH YADAV
7.	1701010001370	VINEET PRATAP SINGH

FEEDBACK FORMS:

1. Ankur Yadav

Feedback form of Value Added Course held on 03rd October 2018-17th October 2018

1. Please rate the course content of Value added course on the factor of 5
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5
2. Rate the course content covered on the parameter of timely delivered
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5
3. Comment on the hands on given in the Value Added Course
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5

Name of the student: Ankur Yadav

Name of the co-ordinator: Rajesh Parihar

2. AVINASH YADAV

Feedback form of Value Added Course held on 03rd October 2018-17th October 2018

1. Please rate the course content of Value added course on the factor of 5
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5
2. Rate the course content covered on the parameter of timely delivered
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5
3. Comment on the hands on given in the Value Added Course
   a) 1
   b) 2
   c) 3
   d) 4
   e) 5

Name of the student: Avinash Yadav

Name of the co-ordinator: Rajesh Parihar